	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	2232	(deposit$3) same silicon same (tungsten adj silicide)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/16 13:08
2	BRS	L2	161	(deposit$3) adj10 silicon adj10 (tungsten adj silicide)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/10/16 13:08

US-PAT-NO: 6251188

DOCUMENT-IDENTIFIER: US 6251188 B1

TITLE: Apparatus for forming laminated thin films or layers

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After formation of the tungsten silicide layer 12, an after-treatment is carried out with the wafer W left disposed on the susceptor 26 (step S4). In the first step, the inner atmosphere of the process vessel 18 is evacuated by vacuum suction. Under this condition, a silane-series gas, e.g., SiH.sub.4 gas, is supplied into the process chamber 20 for a short time, e.g., about 60 seconds, while substantially maintaining the temperature in the step of forming the tungsten silicide layer 12, e.g., 600 to 700.degree. C., so as to **deposit silicon slightly on the surface of the tungsten silicide** layer. The silicon **deposition amount is controlled to form a thin silicon film on the tungsten silicide** layer 12 or to allow silicon flakes to be attached only slightly to the tungsten silicide layer not to form a continuous silicon film. The **deposited silicon permits moderating the stress within the tungsten silicide** layer so as to improve the bonding strength between the polysilicon layer 10 and the tungsten silicide layer 12, as described herein later. Also, the **deposited silicon makes it possible to prevent the tungsten silicide** layer 12 from being attacked by oxygen in the subsequent heat treatment step.

PGPUB-DOCUMENT-NUMBER: 20010052625

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010052625 A1

TITLE: Semiconductor memory device and manufacturing method therefor

PUBLICATION-DATE: December 20, 2001

US-CL-CURRENT: 257/390,438/275 ,438/279

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DATE FILED: June 18, 2001

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	DOC-ID	APPL-DATE
JP	2000-182498	2000JP-2000-182498	June 19, 2000

---------- KWIC ---------

Detail Description Paragraph - DETX:

[0030] Subsequently, the interlayer insulating film 5 is etched after performing photolithography using a code reticule having a uniform pattern density, and ion injection windows are formed on each channel region (see FIG. 1) of the entire memory cell area at a size of 0.18 to 0.24 .mu.m. At the time of etching, since the tungsten silicide films of the interlayer insulating film 5 and the gate electrode 3 have a high selection ratio, the gate electrode 3 is not etched out. However, the thickness of the gate electrode may be reduced in a etching process. It is possible to prevent the etching loss by **depositing a silicon film or a silicon nitride (SiN) film on the**

tungsten silicide film with a thickness of 50 .mu.m. Consequently, the gate electrode can be protected from being converted to a high resistance film due to etching loss, and the ion injection windows can be formed without affecting the gate electrode portion (FIG. 3D).

PGPUB-DOCUMENT-NUMBER: 20010026972

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20010026972 A1

TITLE: Integrated circuit device with MIM capacitance circuit and method of manufacturing the same

PUBLICATION-DATE: October 4, 2001

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APPL-NO: 09/ 805479

DATE FILED: March 13, 2001

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	DOC-ID	APPL-DATE
JP	2000-091744	2000JP-2000-091744	March 29, 2000

---------- KWIC ---------

Detail Description Paragraph - DETX:

[0064] After the above dry etching process, an ammonia-based solution is used to remove resist masks 134, 135. At this time, since silicon layer 203 has been **deposited on the surface of tungsten silicide layer 131, a silicon component is prevented from flowing out of tungsten silicide** layer 131 due to the ammonia-based solution, and hence the silicon concentration in tungsten silicide layer 131 is prevented from being reduced.